Features

- Frequency bands
  - WL1625A: 315MHz, 433MHz
  - WL1625B: 315MHz, 433MHz, 868MHz, 915MHz
- Operating voltage range: 2.4V~5.5V
- 0.5μA deep sleep current with data retention
- Low RX current
  - 4.5mA @ 433MHz
  - 5.8mA @ 868MHz
- Supports FSK modulation
  - FSK support up to 50Ksps symbol rate
- Good reception sensitivity under 0.1% BER (BW=93.6k)
  - -108dBm @ 25Kbps, 433MHz
- Wide RF input power range: from sensitivity to +10dBm
- Support 2-wire I^2C interface for operation configuration
- On-chip VCO and Fractional-N synthesizer with integrated loop filter
- Supports low cost 16MHz crystal
- FCC/ETSI Compliant
- Package type: 10-pin SOP-EP

Applications

- Iron rolling doors
- Ceiling lamps
- Wireless switches
- Drying racks
- Wireless doorbells
- Integrated ceilings
- Other wireless products

General Description

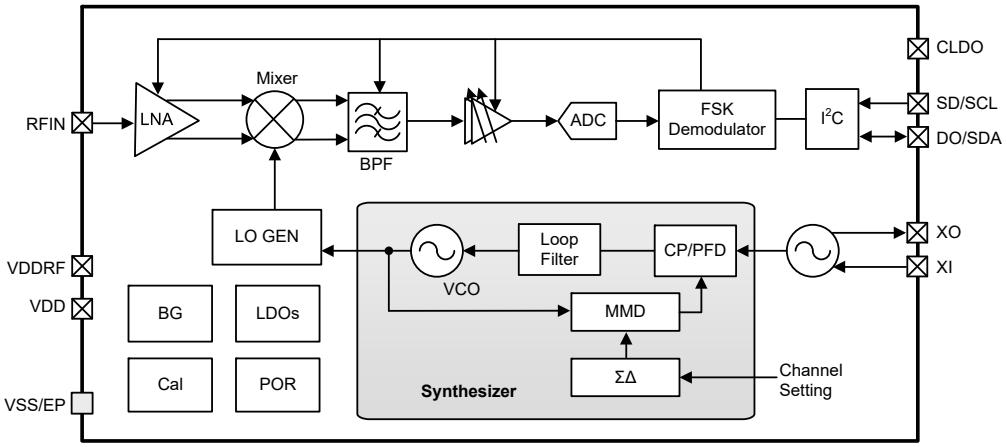
The WL1625x receiver devices adopt a fully-integrated, low-IF FSK receiver with an automatic gain control (AGC) function and a fully-integrated FSK demodulator. The synthesizer is formed by an integrated VCO and a fractional-N PLL to support the 315, 433, 868, and 915MHz frequency bands. The devices only require a crystal and a minimum number of passive components to fully implement a FSK receiver. With this high level of functional integration, these devices provide excellent solutions for low-cost, low power wireless applications.

The devices achieve -112dBm sensitivity for the 433.92MHz bands. They operate from a supply voltage of 2.4V to 5.5V and typically require 4.5mA at 433.92MHz. The devices support a sniff RX mode, where the on/off RX mode function can be controlled by an MCU to achieve a lower than average power consumption using duty RX mode operation.

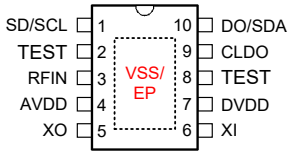
The WL1625 series offers two types of ICs. One is the BC2502A which covers the 315 and 433MHz bands while the BC2502B offers a choice of four frequency bands.

Part Number	Frequency Band
WL1625A	315MHz, 433MHz
WL1625B	315MHz, 433MHz, 868MHz, 915MHz

Block Diagram



Pin Assignment



WL1625A/WL1625B
10 SOP-EP-A

Pin Description

Pin No.	Pin Name	I/O	Description
1	SD/SCL(1)	DI	RX mode shut-down control, should be pulled low in RX Mode
		DI	I²C clock input line in Configuration Mode
2	TEST	—	Not connected, leave floating
3	RFIN	AI	RF LNA input
4	AVDD	PWR	Analog power supply
5	XO	AO	Crystal oscillator output
6	XI	AI	Crystal oscillator input
7	DVDD	PWR	Digital power supply
8	TEST	—	Not connected, leave floating
9	CLDO	PWR	LDO output, connected to a bypass capacitor
10	DO/SDA(1)	DO	Demodulated data output in RX Mode
		DI/DO	I²C data line in Configuration Mode
—	VSS/EP(2)	PWR	Exposed pad, must be connected to ground

Legend: DI: Digital Input; DO: Digital Output; AI: Analog Input;
AO: Analog Output; PWR: Power.

Note: 1. The DO/SDA & SD/SCL pins are default connected to a pull-high resistor after a power on reset. After entering the RX mode, these pull-high resistors are disconnected automatically. An analog debounce function is added to these two pins.

2. The VSS/EP pin located at the exposed pad.

3.The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to 5.5V

Input Digital Voltage ..... V_{SS}-0.3V to V_{DD}+0.3V

Input Analog Voltage ..... V_{SS}-0.3V to 2.1V

Storage Temperature .....-60°C to150°C

Operating Temperature ..... -40°C to 85°C

ESD HBM ..... ±2kV

*Devices being ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=5.0V, f_{XTAL}=16MHz, FSK demodulation with matching circuit, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{OP}	Operating Temperature	—	-40	—	85	°C
V_{DD}	Operating Voltage	—	2.4	5.0	5.5	V
Current Consumption						
I_{SLP}	Current Consumption, Deep Sleep Mode	—	—	0.5	—	μA
I_{RX}	Current Consumption, RX Mode	@ 315MHz	—	4.7	—	mA
		@ 433MHz	—	4.5	—	
		@ 868MHz	—	5.8	—	
		@ 915MHz	—	5.8	—	
R_{PH}	Pull-high Resistance for I/O Ports	—	—	100	—	kΩ

A.C. Characteristics

Ta=25°C, V_{DD}=5.0V, f_{XTAL}=16MHz, FSK demodulation with matching circuit, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Receiver Characteristics						
f_{RF}	RF Frequency Range	WL1625A/WL1625B	—	315	—	MHz
		WL1625A/WL1625B	—	433.92	—	
		WL1625B only	—	868.35	—	
		WL1625B only	—	915	—	
SR	Symbol Rate	—	1	—	50	Ksps
f_{DEV}	Frequency Deviation	—	4	—	25	kHz
P_{SENS}(1)	RX Sensitivity – 315MHz (Instrument: Keysight E4438C)	SR=1Ksps, BER=0.1%	—	-105	—	dBm
		SR=10Ksps, BER=0.1%	—	-108	—	
	RX Sensitivity – 433.92MHz (Instrument: Keysight E4438C)	SR=1Ksps, BER=0.1%	—	-106	—	
		SR=10Ksps, BER=0.1%	—	-108	—	
	RX Sensitivity – 868.35MHz (Instrument: Keysight E4438C)	SR=5Ksps, BER=0.1%	—	-105	—	
		SR=10Ksps, BER=0.1%	—	-105	—	
	RX Sensitivity – 915MHz (Instrument: Keysight E4438C)	SR=5Ksps, BER=0.1%	—	-104	—	
		SR=10Ksps, BER=0.1%	—	-104	—	
SE_{RX}	Receiver Spurious Emission	25MHz~1GHz	—	—	-57	dBm
		Above 1GHz	—	—	-47	
	Blocking Immunity	±2MHz offset	—	40	—	dBc
		±10MHz offset	—	64	—	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Cof_{ST}	Configure Mode Settling Time (Deep Sleep to Configure Mode)	49US XO	—	1.5	—	ms
		SMD3225 XO	—	2.5	—	ms
RX_{ST}	RX Mode Settling Time (Deep Sleep Mode to RX Mode Data Out)	49US XO	—	1.5	—	ms
		SMD3225 XO	—	2.5	—	ms
LO Characteristics						
f_{LO}	Frequency Coverage Range	WL1625A/WL1625B	300	—	360	MHz
		WL1625A/WL1625B	390	—	450	
		WL1625B only	850	—	935	
	Frequency Resolution	—	—	—	0.1	kHz
	Synthesizer Locking Time	—	—	130	—	μs
Crystal Oscillator Characteristics						
f_{XTAL}	Crystal Frequency	General case	—	16	—	MHz
t_{SU}	X'tal Startup Time(2)	49US XO	—	0.5	—	ms
		SMD3225 XO	—	1.5	—	ms
ESR	X'tal Equivalent Series Resistance	—	—	—	100	Ω
C_L	X'tal Load Capacitance	—	—	16	—	pF
TOL	X'tal Tolerance(3)	—	-20	—	+20	ppm

Note: 1. 315/433MHz Bands Digital Filter BW=93.6kHz
868/915MHz Bands Digital Filter BW=187.2kHz

2. The X'tal startup time depends on crystal property.

3. This is the total tolerance including (1) Initial tolerance (2) Crystal loading (3) Aging (4) Temperature dependence.

I²C Characteristics

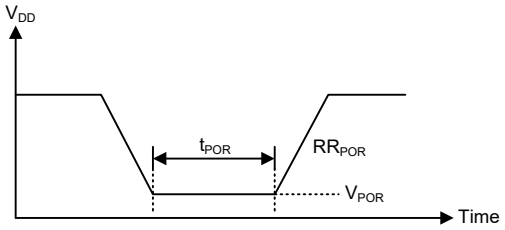
Ta=-40°C~85°C, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	Serial Clock Frequency	—	—	—	1	MHz
t_{BUF}	Bus Free Time between Stop and Start Condition	SCL=1MHz	250	—	—	ns
t_{LOW}	SCL Low Time	SCL=1MHz	500	—	—	ns
t_{HIGH}	SCL High Time	SCL=1MHz	500	—	—	ns
$t_{su(DAT)}$	Data Setup Time	SCL=1MHz	100	—	—	ns
$t_{su(STA)}$	Start Condition Setup Time	SCL=1MHz	250	—	—	ns
$t_{su(STO)}$	Stop Condition Setup Time	SCL=1MHz	250	—	—	ns
$t_{h(DAT)}$	Data Hold Time	SCL=1MHz	100	—	—	ns
$t_{h(STA)}$	Start Condition Hold Time	SCL=1MHz	250	—	—	ns
$t_{r(SCL)}$	Rise Time of SCL Signal	SCL=1MHz	—	—	100	ns
$t_{f(SCL)}$	Fall Time of SCL Signal	SCL=1MHz	—	—	100	ns
$t_{r(SDA)}$	Rise Time of SDA Signal	SCL=1MHz	—	—	100	ns
$t_{f(SDA)}$	Fall Time of SDA Signal	SCL=1MHz	—	—	100	ns

Power on Reset Characteristics

Ta=25°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	1	—	—	ms



Functional Description

The WL1625x devices are ultra-low power, high performance, low-cost FSK receivers suitable for use in wireless applications with a frequency of 315, 433, 868, 915MHz respectively. The devices are formed by a low-IF receiver, followed by a FSK demodulator and a fractional-N synthesizer. They only require a crystal and a minimum number of passive components to implement a FSK receiver.

FSK RF Receiver

The WL1625x devices adopt a fully-integrated, low-IF receiver architecture. The received RF signal is first amplified by a low noise amplifier (LNA), after which the frequency is reduced to an intermediate frequency (IF). The IF signal is filtered by a channel-selected filter which rejects the unwanted out-of-band interference signals and image signal. After the BPF stage, the desired IF signal is amplified by the limiter amplifier which generates a received-signal-strength-indicator (RSSI) signal.

The devices feature an automatic gain control (AGC) unit which adjusts the front-end gain according to the RSSI. The AGC can increase the dynamic range of the RSSI and enable the devices to receive a wide dynamic range RF signal.

The FSK one/zero type data is generated by comparing the RSSI signal to a manipulated threshold. This threshold is crucial to the performance of FSK demodulation. The agile threshold detection mechanism can reduce glitches when there is no RF signal or when long zero data streams are received. It also includes a fast tracking threshold to offer good immunity from co-channel interferences.

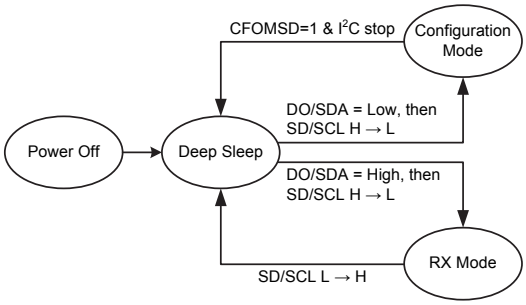
Operation Modes

The devices provide four operation modes, power off mode, deep sleep mode, RX mode and configuration mode.

In the deep sleep mode, there is less than 1μA of sleep mode leakage current with register data retention.

In the RX Mode, the devices execute normal RX operations that receive incoming RF signals from the antenna and then output the demodulated data onto the DO/SDA pin.

In the Configuration Mode, the devices are operated as I^2C slaves and are programmed by an external MCU. Users can select the desired RX channel by configuring the internal registers. After the configuration has completed, the devices will return to the deep sleep mode by setting the CFOMSD bit high.



Operation Mode Switching

Note: The CFOMSD bit will be cleared to zero automatically when the device leaves the configuration mode.

Sniff RX Mode

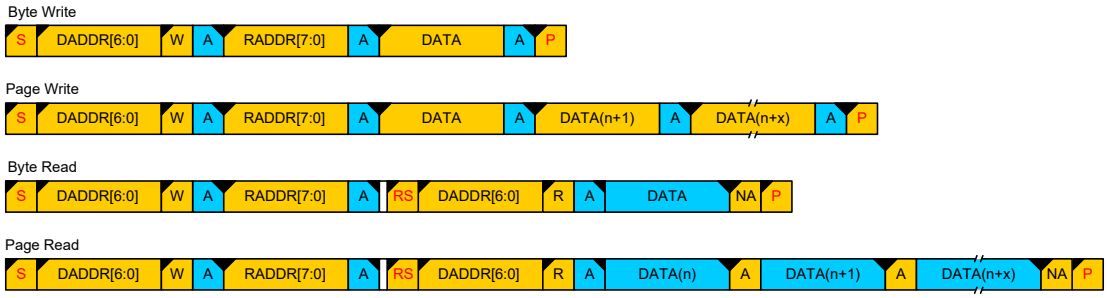
The devices also provide a Sniff RX mode as it is controlled by an MCU. The SD/SCL pin defaults to a pull-high state. After power-on the devices will enter the deep sleep mode. An MCU could control the SD/SCL pin to make it enter or leave the RX mode. With additional SD/SCL control, users can optimize the average power consumption based on their applications.

Configuration Mode

The devices include an I²C serial interface, which is used for bidirectional, two-line communication between multiple I²C devices. The two lines of this interface are the serial data line, SDA, and the serial clock line, SCL. Both lines are equipped with de-bounce functions. After a power on reset, these two pins are pulled to DVDD by default using internal pull-high resistors. When entering the RX mode, the pull-high resistors are disconnected.

The devices support the I²C format for byte write, page write, byte read and page read formats. Every byte placed onto the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.

It should be noted that the I²C is a non-standard I²C interface, which only supports a single device for connection.



Bus Direction: : Host to device; : Device to host;

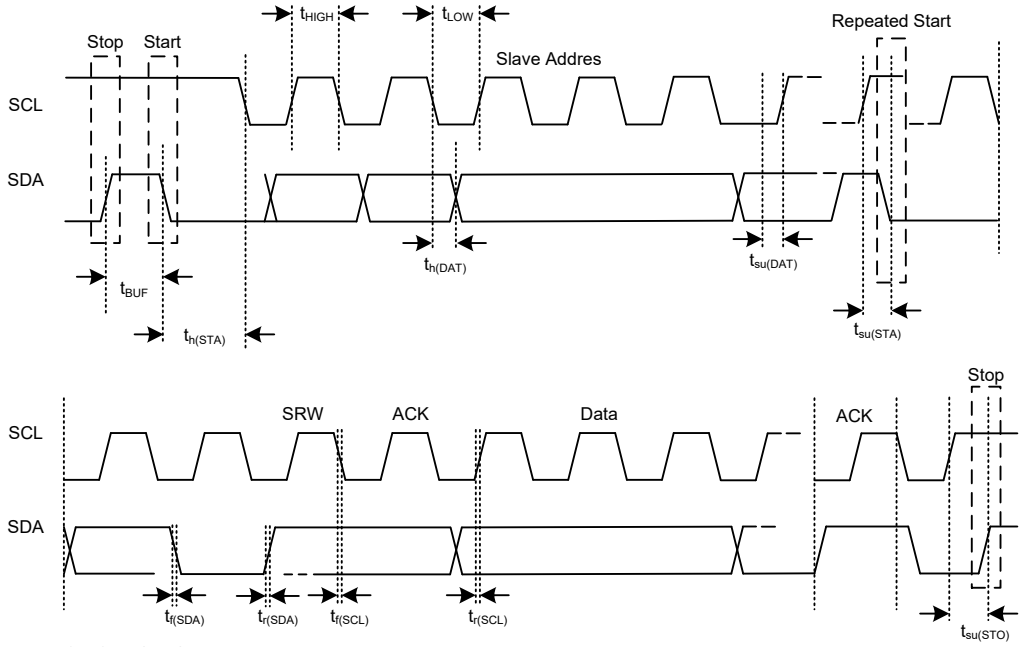
Symbol Definitions: S: Start; RS: Repeated Start; P: Stop;

DADDR[6:0]: Device Address, 25h;

R:Read(1); W: Write(0);

RADDR[7:0]: register address;

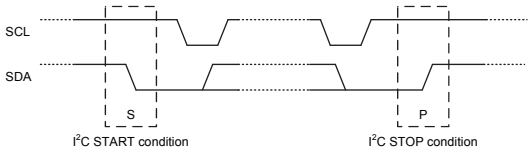
A: ACK(0); NA: NAK(1)



S = Start (1 bit)
SA = Slave Address (7 bits)
SR = SRW bit (1 bit)
M = Slave device send acknowledge bit (1 bit)
D = Data (8 bits)
A = ACK (RXAK bit for transmitter, TXAK for receiver, 1 bit)
P = Stop (1 bit)

I²C Communication Timing Diagram

I²C START and STOP Conditions

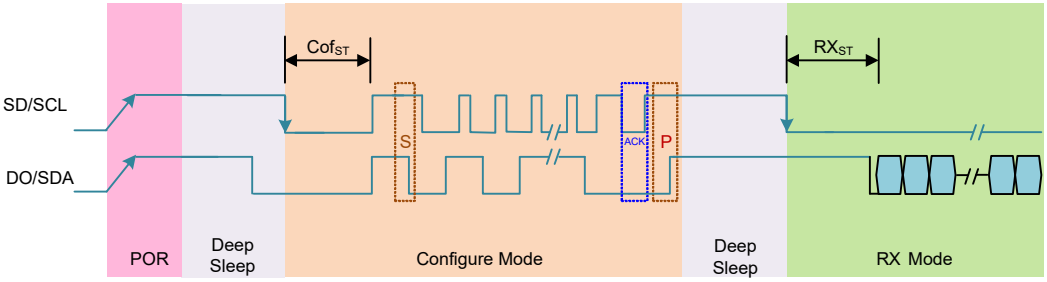


- A high to low transition on the SDA line while SCL is high defines a START condition.
- A low to high transition on the SDA line while SCL is high defines a STOP condition.
- START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again a certain time after the STOP condition.
- The bus remains busy if a Repeated START (RS) is generated instead of a STOP condition. The START (S) and Repeated START (RS) conditions are functionally identical.

Configuration Mode Switching and Timing

As shown in the following diagram, when SDA is low and a SCL falling edge occurs, the device changes from the Deep Sleep Mode to the Configuration Mode after a 1.5ms delay time. If the SCL level remains high for a time greater than or equal to 20ms, the device will be forced to leave the Configuration Mode.

If the devices are connected to an MCU through an I²C interface, users can set the CFOMSD bit of the register, at address 40h, to leave the Configuration Mode.



Entering and Leaving Configuration Mode Timing Diagram

Register Map

When connected to an external MCU, the device's RF frequency can be setup using a series of internal registers in the Configuration Mode. The register data is written to and read from the devices using their internal I²C interface. The following provides a summary of all internal registers and their detailed descriptions.

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
00h	—	Reserved							
05h	FSKDM1	Reserved						MDIV_SEL [1:0]	
06h	—	Reserved							
07h	—	Reserved							
09h	—	Reserved							
0Ah	—	Reserved							
10h	OM	—	BAND_SEL[1:0]		—	—	—	—	—
11h	—	Reserved							
12h	SX1	—	D_N[6:0]						
13h	SX2	D_K[7:0]							
14h	SX3	D_K[15:8]							
15h	SX4	—	—	—	—	D_K[19:16]			
1Bh	—	Reserved							
1Fh	—	Reserved							
32h	—	Reserved							
40h	I2C1	Reserved							CFOMSD
43h	—	Reserved							
46h	—	Reserved							

Note: The addresses which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The recommended values for the registers are listed below:

Addr.	Setting	Addr.	Setting
00h	60h	1Bh	2Fh
06h	71h	1Fh	10h
07h	07h	32h	82h
09h	7Fh	43h	315MHz Band: 84h 433/868/915MHz Bands: 80h
0Ah	7Fh	46h	01h
11h	69h		

- **FSKDM1 – FSK De-Modulator Control Register 1 (Addr: 05H)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	MDIV_SEL [1:0]	
R/W	—	—	—	—	—	—	R/W	
POR	1	0	0	0	0	0	0	1

Bit 7~2 Reserved bit, cannot be changed

Bit 1~0 **MDIV_SEL[1:0]**: Demodulator operation clock divider selection

00: 187.2kHz

01: 93.6kHz

10: 46.8kHz

11: reserved

- **OM – Operation Mode Control Register (Addr: 10H)**

Bit	7	6	5	4	3	2	1	0
Name	—	BAND_SEL[1:0]		—	—	—	—	—
R/W	—	R/W		—	—	—	—	—
POR	0	0	0	0	0	0	0	0

Bit 7 Reserved bit, cannot be changed

Bit 6~5 **BAND_SEL[1:0]**: Band selection

00: 300~360MHz Band

01: 390~450MHz Band

10: Reserved

11: 850~935MHz Band (BC2502B Only)

Bit 4~0 Reserved bit, cannot be changed

- **SX1 – Fractional-N Synthesizer Control Register 1 (Addr: 12H)**

Bit	7	6	5	4	3	2	1	0
Name	—	D_N[6:0]						
R/W	—	R/W						
POR	1	0	1	0	1	0	1	1

Bit 7 Reserved bit, must be set “1”

Bit 6~0 **D_N[6:0]**: RF channel frequency integer number code

$D\_N[6:0]=\text{Floor}\left(\frac{f_{RF}-f_{IF}}{f_{XTAL}}\times 0.8\right)\times M$, (315MHz: M=2, Other Bands: M=1)

For example:

f_{XTAL}=16MHz, RF channel frequency(f_{RF})=315MHz, Intermediate Frequency (f_{IF})=200kHz

→ (315MHz-0.2MHz)/(16MHz)×0.8×2=31.48

→ D_N=31

→ Dec2Bin(31)=001_1111

f_{XTAL}=16MHz, RF channel frequency(f_{RF})=433.92MHz, Intermediate Frequency (f_{IF})=200kHz

→ (433.92MHz-0.2MHz)/(16MHz)×0.8=21.686

→ D_N=21

→ Dec2Bin(21)=001_0101

- **SX2 – Fractional-N Synthesizer Control Register 2 (Addr: 13H)**

Bit	7	6	5	4	3	2	1	0
Name	D_K[7:0]							
R/W	R/W							
POR	1	0	1	1	0	1	1	1

Bit 7~0 **D_K[7:0]**: RF channel frequency fractional number code lowest byte

- **SX3 – Fractional-N Synthesizer Control Register 3 (Addr: 14H)**

Bit	7	6	5	4	3	2	1	0
Name	D_K[15:8]							
R/W	R/W							
POR	1	1	1	1	0	0	1	1

Bit 7~0 **D_K[15:8]**: RF channel frequency fractional number code medium byte

- **SX4 – Fractional-N Synthesizer Control Register 4 (Addr: 15H)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	D_K[19:16]			
R/W	—	—	—	—	R/W			
POR	0	1	1	0	0	1	0	1

Bit 7~4 Reserved bit, cannot be changed

Bit 3~0 **D_K[19:16]**: RF channel frequency fractional number code highest byte

$D\_K[19:0]=Floor\ \{(\frac{f_{RF}-f_{IF}}{f_{XTAL}}\times 0.8\times M - D\_N[6:0]\times 2^{20}\}$, (315MHz: M=2, Other Bands: M=1)

For example:

f_{XTAL}=16MHz, RF channel frequency(f_{RF})=315MHz, Intermediate Frequency (f_{IF})=200kHz

→ (315MHz-0.2MHz)/(16MHz)×0.8×2=31.48

→ D_K=0.48×2^{20}=503316

→ Dec2Bin(503316)=0111_1010_1110_0001_0100

f_{XTAL}=16MHz, RF channel frequency(f_{RF})=433.92MHz, Intermediate Frequency (f_{IF})=200kHz

→ (433.92MHz-0.2MHz)/(16MHz)×0.8=21.686

→ D_K=0.686×2^{20}=719323

→ Dec2Bin(719323)=1010_1111_1001_1101_1011

- **I2C1 – I²C Control Register 1 (Addr: 40H)**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	CFOMSD
R/W	—	—	—	—	—	—	—	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~1 Reserved bit, cannot be changed

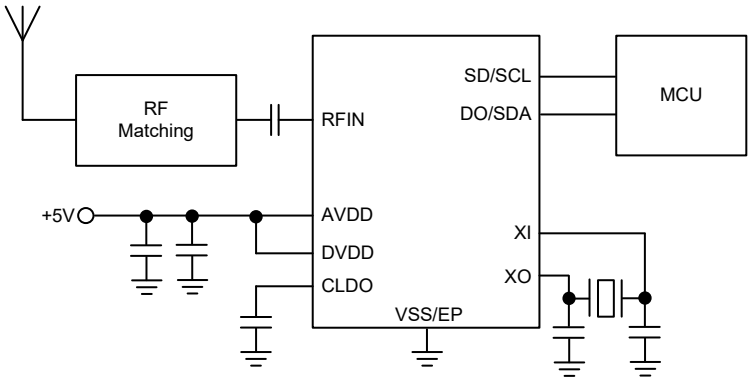
Bit 0 **CFOMSD**: Configuration Mode shut down control

0: No operation

1: Exit Configuration Mode

In the configuration mode the devices can be forced to leave this mode by first setting the CFOMSD bit high and then followed by an I²C stop condition. After leaving the Configuration Mode the CFOMSD bit will be reset to zero automatically.

Application Circuits



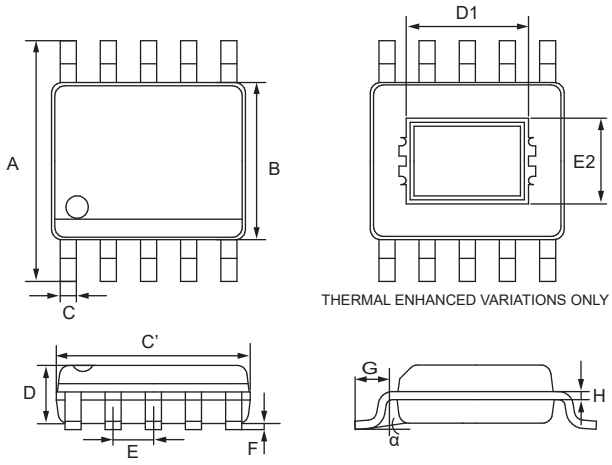
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

10-pin SOP-EP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.018
C′	—	0.193 BSC	—
D	—	—	0.069
D1	0.059	—	—
E	—	0.039 BSC	—
E2	0.039	—	—
F	0.000	—	0.006
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.0 BSC	—
B	—	3.9 BSC	—
C	0.30	—	0.45
C′	—	4.9 BSC	—
D	—	—	1.75
D1	1.50	—	—
E	—	1.0 BSC	—
E2	1.00	—	—
F	0.00	—	0.15
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°